Application No.: 09/991,142 Docket No.: 21806-00134-US

AMENDMENTS TO THE CLAIMS

This listing of the claims will replace all prior versions and listing of the claims in this application.

Listing of the Claims:

1. (Previously presented) A semiconductor wafer comprising:

a first semiconductor device having a first subcollector; and

a second semiconductor device having a second subcollector, wherein the second subcollector differs from said first subcollector, having a sheet resistance exceeding 50 Ω/square to provide lateral ballasting of said second subcollector for providing ESD protection.

2. (Previously presented) The semiconductor wafer as recited in claim 1, wherein said second subcollector differs from said first subcollector in impurity type.

3. (Currently amended) The semiconductor wafer as recited in claim ~~2~~ 1, wherein said first subcollector comprises an arsenic impurity and said second subcollector comprises an antimony impurity.

4. (Original) The semiconductor wafer as recited in claim 2, wherein said first subcollector comprises an implant dose in the $1x10^{16}cm^{-2}$ range and said second subcollector comprises an implant dose in the $1x10^{15}cm^{-2}$ range.

5. (Currently amended) The semiconductor wafer as recited in claim 1, wherein said second subcollector provides a higher resistance and a higher breakdown voltage (BV_{CEO}, BV_{CBO}) than said first subcollector.

6. (Original) The semiconductor wafer as recited in claim 1, wherein said first subcollector has a sheet resistance below approximately 20 Ω/square, and said second subcollector has a sheet resistance above approximately 50 Ω/square.

7. (Original) The semiconductor wafer as recited in claim 1, wherein said first subcollector is part of a bipolar transistor, a Schottky barrier diode, a PIN diode, a p+/subcollector diode, a p+/n-well/subcollector diode, a pn diode, or a varactor.

8. (Original) The semiconductor wafer as recited in claim 1, further comprising an additional diffusion abutting said first subcollector.

9. (Original) The semiconductor wafer as recited in claim 8, wherein said additional diffusion is a pedestal implant or a reach through diffusion.

10. (Original) The semiconductor wafer as recited in claim 1, wherein said first subcollector has an edge defined by a deep trench.

11. Cancelled.

12. (Original) The semiconductor wafer as recited in claim 1, wherein said first device is a first transistor and said second device is a second transistor.

13. (Currently amended) First and second bipolar transistors formed on a p-substrate, said first transistor comprising:

a Sb subcollector;

a n-epi collector;

a SiGe polysilicon p-doped extrinsic base;

a SiGe silicon single crystal intrinsic base; and

said second transistor comprising:

an As subcollector having a sheet resistance ~~exceeding 50 Ω/square~~ at 50-200 Ω/square;

a n-epi collector;

a SiGe polysilicon extrinsic base; and

a SiGe single crystal extrinsic base, said second transistor providing ESD protection as a result of the selection of As as a subcollector which provides for lateral ballasting.

14. (Original) The semiconductor structure of claim 13, further comprising a polysilicon emitter.

15. Cancelled.

16. (Withdrawn) A method for manufacturing a semiconductor device on a wafer comprising the following steps:

forming a first subcollector region in the wafer;

forming a second subcollector region in the wafer; wherein the second subcollector differs from the first subcollector;

forming an isolation structure abutting an end portion of at least one subcollector region;

forming a SiGe film or SiGeC film on the wafer surface above said first and second subcollector regions for formation of a transistor base region;

forming an emitter structure on the SiGe or SiGeC film.

17. (Withdrawn) The method of manufacturing a semiconductor device of Claim 16, wherein the first subcollector implant differs from the second subcollector region in impurity type or doping concentration.

18. (Withdrawn) The method of manufacturing a semiconductor device of Claim 16, wherein a first bipolar transistor is formed on said first subcollector region and a second bipolar transistor is formed on said second subcollector region.

19. (Withdrawn) A method of manufacturing a semiconductor device on a wafer comprising the following steps:

forming a subcollector region by implantation of the wafer with a first dopant and with a second dopant;

forming an isolation structure on the subcollector region;

forming a SiGe film or SiGeC film on the wafer surface for formation of a transistor base region;

forming an emitter structure on the SiGe or SiGeC film.

20. (Currently amended) The semiconductor wafer of claim 1, wherein said second subcollector has a different doping concentration ~~of the same impurity~~ than said first subcollector, thereby increasing said second semiconductor device ESD robustness over the ESD robustness of said first semiconductor device.

21. (Previously presented) The semiconductor wafer of claim 1, wherein said first device is a bipolar transistor having a subcollector doping selected to enhance said transistor performance, and said second semiconductor device has a doping selected to enhance its ESD performance.

22. (Currently amended) The semiconductor wafer according to claim 20, wherein said second semiconductor device is [formed] biased to discharge an ESD voltage.